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10/784,494	02/23/2004	Satoshi Machida	S004-5216	2129

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ADAMS & WILKS
31st Floor
50 Broadway
New York, NY 10004

EXAMINER	
WYATT, KEVIN S	

ART UNIT	PAPER NUMBER
2878	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,494	MACHIDA, SATOSHI	
	Examiner	Art Unit	
	Kevin Wyatt	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *13-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 13-18 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 12/12/2005.

2. Applicant's election with traverse of Group II, claims 1-12 and 19-20 in the reply filed on 12/12/2005 is acknowledged. The traversal is on the ground(s) that claims 1-12 and 19-20 are readable on the elected invention. This is not found persuasive because, the claims of Group I lack the subtracter, clamp circuit and the gain amplifier provided in Group II. Therefore, the claims of Group II are distinct and have separate utility from Group I.

The requirement is still deemed proper and is therefore made FINAL.

Claim Objections

3. Claim 19 is objected to because of the following informalities:

In claim 19, lines 2-3, "receiving its input an input" should be changed to --receiving as its input, an input --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-2, and 8-9, and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 3-6, the recited limitation "a time interval of the first half and for a time interval of the second half for the time interval of the first half" is unclear because it indicates that the time interval of the first half is further divided into two additional parts. Further clarification of this limitation is needed.

In claim 2, lines 4-5, the recited limitation "a reference signal becoming a reference" does not indicate or what type of signal comprises the reference signal or which from which circuit does it originate.

In claim 8-9, lines 5-6, and claim 10, lines 20-21, the recited limitation "the reference signal becoming a reference" does not indicate or what type of signal comprises the reference signal or which from which circuit does it originate.

All claims dependent upon the claims above also inherit the indefiniteness of the indicated claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 6-9, and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Fossum (U.S. Patent No. 5,841,126).

Regarding claim 1, Fossum shows in Figs. 5A-B a signal processing circuit (column circuit), comprising: a sample/hold circuit (combination of first and second holding capacitors 510 and 512) for sampling an input signal separately inputted for a time interval of the first half and for a time interval of the second half for the time interval of the first half and for holding the inputted signal for the time interval of the second half (col. 5, lines 58-68); a subtracter (combination of DDS (520), COL (522 and 524)) for taking a difference between the sampled and held signal and the inputted signal; and a voltage clamp circuit (transistors 550 and 552) for receiving as its input a signal from the subtracter, wherein the voltage clamp circuit carries out clamping for a part of or all of the time interval if the first half (col. 6, lines 35-39, and lines 46-51).

Regarding claim 2, Fossum shows in Figs. 1, and 5A-B a signal processing circuit which receives as its input an optical signal obtained due to storage of electric charges generated due to light incident upon photoelectric charges generated due to light incident upon photoelectric converter, and a reference signal becoming a reference for the photoelectric converter (col. 3, lines 5-21), wherein the optical signal is inputted for the time interval of the first half and reference signal (reset noise) is inputted of the time interval of the second half, or the first half and the optical signal is inputted for the time interval of the second half (col. 6, lines 23-34).

Regarding claim 3, Fossum shows in Fig. 5B a circuit (output driver circuit (554 and 556)) for sampling a signal from the voltage clamp circuit for the time interval of the second half to hold the sampled signal.

Regarding claim 6, Fossum shows in Figs. 5A-B an image sensor IC, comprising the signal processing circuit as claimed in claim 2, which is formed together with photoelectric converter on one semiconductor substrate.

Regarding claim 7, Fossum shows in Figs. 5A-B an image sensor, comprising the signal processing circuit (column circuit) and the photoelectric converter (pixel) as claimed in claim 2.

Regarding claim 8, Fossum shows in Figs. 5A-B an image sensor, comprising: read means (504, photodiode) for reading out an optical signal and a reference signal (reset noise) to a common signal line, wherein the optical signal is obtained due to storage of electric charges generated due to light incident upon photoelectric converter (col. 5, lines 40-43) and the reference signal (reset noise) is becoming a reference for the photoelectric converter (column circuit); a sample/hold circuit (capacitors 510 and 512) for receiving as its input a signal from the common signal line; and a subtracter (combination of DDS (520), COL (522 and 524)) for taking and amplifying a difference between the sampled and held signal and the inputted signal (col. 6, lines 51-58).

Regarding claim 9, Fossum shows in Figs. 5A-B an image sensor, comprising: a first hold circuit for holding an optical signal (combination of photodiode (502) and follower (508)) obtained due to storage of electric charges generated due to light incident upon photoelectric converter (col. 5, lines 40-43); a second hold circuit for

holding a reference signal becoming a reference for the photoelectric converter (column circuit); read means (514, i.e., row select transistor) for reading out the optical signal and the reference signal which are held in order to a common signal line; a sample/hold circuit for receiving as its input a signal from the common signal line (capacitors 510 and 512); and a subtracter (combination of DDS (520), COL (522 and 524)) for taking and amplifying a difference between the sampled and held signal and the inputted signal (col. 6, lines 51-58).

Regarding claim 19, Fossum shows in Figs. 5A-B a signal processing method for use in a signal processing circuit comprising at least: a sample/hold circuit (combination of first and second holding capacitors 510 and 512) for receiving its input an input signal having a time interval of the first half and a time interval of the second half (col. 5, lines 58-68); a subtracter (combination of DDS (520), COL (522 and 524)) for receiving as its input a signal from the sample/hold circuit and the input signal; and a voltage clamp circuit (transistors 550 and 552) for receiving as its input a signal from the subtracter and a reference voltage, wherein: the sample/hold circuit (combination of first and second holding capacitors 510 and 512), for the time interval of the first half of the input signal, holds the input signal and outputs the held input signal to the subtracter (col. 8, lines 57-59); the subtracter (combination of DDS (520), COL (522 and 524)), for the time interval of the second half of the input signal, outputs a difference signal exhibiting a difference between a signal from the sample/hold circuit and the input signal to the clamp circuit (col. 8, lines 64-66 and col. 9, lines 27-31); and the voltage clamp circuit (transistors 550 and 552), for the time interval of the first half, clamps an output signal of

the voltage clamp circuit to the reference voltage, and for the time interval of the second half, superimposes the difference signal on the reference voltage (col. 6, lines 46-58).

Regarding claim 20, Fossum shows in Figs. 5A-B a signal processing method according to claim 19, wherein an output signal from the sample/hold circuit and the input signal are amplified to be inputted to the subtracter.

8. Claims 1, 4-5, and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Sauer (U.S. Patent No. 6,320,616 B1).

Regarding claim 1, Sauer shows in Fig .1, a signal processing circuit (150), comprising: a sample/hold circuit (combination of transistor (SH), C1 and C2) for sampling an input signal separately inputted for a time interval of the first half and for a time interval of the second half for the time interval of the first half and for holding the inputted signal for the time interval of the second half: a subtracter (combination of node (157) and node (156), col. 5, lines 16-28) for taking a difference between the sampled and held signal and the inputted signal; and a voltage clamp circuit (gate of transistor (M5), clamp line (CL)) for receiving as its input a signal for the subtracter, wherein the voltage clamp circuit carries out clamping for a part of or all of the time interval if the first half.

Regarding claim 4, Sauer shows in Fig .1, a gain amplifier (combination of transistor (M6), and buffer) for amplifying a signal from the voltage clamp circuit (gate of transistor (M5), clamp line (CL)), wherein a reference voltage (reset noise) for the gain amplifier and a first reference voltage used to carry out the clamping in the voltage clamp circuit are common to each other (col. 4, line 55-60).

Regarding claim 5, Sauer shows in Fig .1, that a reference voltage (reset noise) for the subtracter and a first reference voltage used to carry out the clamping in the voltage clamp circuit are common to each other (the voltage taken from R1 COL_READ (X)).

Regarding claim 10, Sauer shows in Fig .1 an image sensor, comprising: a photoelectric converter (110, i.e., APS pixel); a signal processing circuit (150) for receiving as its input a signal of the photoelectric converter; a signal output terminal (source terminal of M3) connected to an input terminal of the signal processing circuit (150); a reference voltage terminal (COL_READ (X) line) connected to a terminal at which a reference voltage for the signal processing circuit appears; a reference voltage circuit (load transistor (MN1)); and a resistor (R1) provided between the reference voltage circuit (load transistor (MN1)) and the reference voltage terminal (COL_READ (X) line), the signal processing circuit comprising: a sample/hold circuit (combination of transistor (SH), C1 and C2) for separately receiving as its input an optical signal and a reference signal for a time interval of the first half and for a time interval of the second half to sample the inputted signal for the time interval of the second half, wherein the optical signal for the time interval of the second half, wherein the optical signal is obtained due to storage of electric charges generated due to light incident upon a photoelectric conversion area (116, i.e., photodetector) of the photoelectric converter (110, i.e., APS pixel) and the reference signal (COL_READ (X) line) is becoming a reference for the photoelectric converter; a subtracter (combination of node (157) and node (156), col. 5, lines 16-28) for taking a difference between the sampled and held

signal and the inputted signal; and a voltage clamp circuit (gate of transistor (M5), clamp line (CL)) for clamping a signal from the subtracter for the time interval of the first half, wherein of a reference voltage for the voltage clamp circuit and a reference voltage for the subtracter is supplied through the reference voltage terminal.

Regarding claim 11, a plurality of image sensor ICs (one of a 640(H)x480(V) APS array) each as claimed in claim10, wherein reference voltage terminals of the plurality of image sensor ICs are electrically connected to one another (col.2, lines 47-54).

Regarding claim 12, An image sensor IC according to claim 10, further comprising a gain amplifier (combination of transistor (M6), and buffer) for amplifying the clamped signal, wherein a reference voltage for the gain amplifier (combination of transistor (M6), and buffer, col. 4, line 55-60) is supplied through the reference voltage terminal.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fossum (U.S. Patent No. 5,949,483) discloses an active pixel sensor array with multireolution readout.

Kokubun (Publication No. U.S. 2003/0146369 A1) discloses a correlated double sampling circuit and CMOS image sensor including the same.

Machida (Publication No. U.S. 2002/0166949 A1) discloses a photoelectric converter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Wyatt whose telephone number is (571)-272-5974. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571)-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.W.

Georgia Epps
Supervisory Patent Examiner
Technology Center 2800